What is claimed is:

1. A high voltage control circuit for used in a semiconductor device, comprising:

an external voltage detector for receiving an external supply voltage to generate a low voltage signal in case that the external supply voltage level is under a predetermined voltage level;

a voltage level detector for receiving a high voltage activates a word line to sensing the high voltage level and generating a generator enabling signal in case that the high voltage level is under a reference voltage level, wherein the larger reference voltage level is increased in response to the low voltage signal is inputted from the external voltage detector;

a generator for receiving the generator enabling signal and the low voltage signal to generate a periodic signal in response to the generator enabling signal and the low voltage signal; and

a pump for generating a newly adjusted high voltage in response to the periodic signal.

2. The high voltage control circuit as recited in claim 1, wherein the external voltage detector includes:

a first resistor coupled to a word line operating voltage for serving as a constant current source;

a first NMOS transistor diode-connected for serving as a

diode, its drain being coupled to the first resistor and its gate;

a second NMOS transistor diode-connected for serving as a diode, its drain being coupled to its gate and source of the first NMOS transistor and its source being coupled to a ground voltage;

a differential amplifier for comparing two voltages supplied at first and second input terminals and outputting either a second logical signal if the voltage supplied at the first input terminal is larger than the other or a first logical signal if the voltage supplied at the second input terminal is larger than the other, wherein a first input terminal of the differential amplifier is coupled to the drain of the first NMOS transistor and a second input terminal is coupled to the external supply voltage, and wherein the second logical signal is characterized by the first logical signal;

a first inverter for receiving and inverting an output signal of the differential amplifier; and

a second inverter for receiving and inversing an output signal of the first inverter and outputting it as the low voltage signal to the voltage level detector and the generator.

3. The high voltage control circuit as recited in claim 1, wherein the voltage level detector includes:

a third inverter for receiving and inversing the low voltage signal from the external voltage detector;

a third NMOS transistor for receiving an output signal

of the third inverter at its gate, its drain being coupled to the word line operating voltage;

a second resistor of which each side is individually coupled to the drain of the third NMOS transistor and the source of the third NMOS transistor;

a third resistor coupled to the second resistor;

a forth resistor of which each side is individually coupled to the third resistor and the ground voltage;

a differential amplifier for comparing two voltages supplied at first and second input terminals and outputting either a second logical signal if the voltage supplied at the first input terminal is larger than the other or a first logical signal if the voltage supplied at the second input terminal is larger than the other, wherin its first input terminal is coupled to the third resistor and its second input terminal is coupled to a core supply voltage, and wherein the second logical signal is characterized by the first logical signal;

a forth inverter for receiving and inverting an output signal of the differential amplifier; and

a fifth inverter for receiving and inverting an output signal of the forth inverter and outputting the inverted output signal as the generator enabling signal to the generator.

4. The high voltage control circuit as recited in claim 1, wherein the generator includes:

a first generating logic for generating a first generating signal in case that the low voltage signal is not activated;

a second generating logic for generating a second generating signal in case that the low voltage signal is activated, a period of the second generating signal being longer than that of the first generating signal;

a NOR gate for carrying out a NOR operation after receiving output signals of the first and second generating logics; and

a sixth inverter for outputting the periodic signal after receiving and inversing an output signal of the NOR gate.

5. The high voltage control circuit as recited in claim 4, wherein the first generating logic includes:

a first NAND gate for carrying out a NAND operation after receiving several signals which at least include the low voltage signal and the generator enabling signal;

a seventh inverter for receiving and inversing an output signal of the first NAND gate;

a eighth inverter for receiving and inversing an output signal of the seventh inverter;

a ninth inverter for receiving and inversing an output signal of the eighth inverter;

a tenth inverter for receiving and inversing an output signal of the ninth inverter and thereon outputting to the first NAND gate; and

a eleventh inverter for receiving and inversing an output signal of the tenth inverter and outputting a periodic signal to the NOR gate.

6. The high voltage control circuit as recited in claim 4, wherein the second generating logic includes:

a twelfth inverter for receiving and inversing the low voltage signal;

a second NAND gate for carrying out a NAND operation after receiving several signals which at least include the low voltage signal and the generator enabling signal;

a thirteenth inverter for receiving and inversing an output signal of the second NAND gate;

a fourteenth inverter for receiving and inversing an output signal of the thirteenth inverter;

a fifteenth inverter for receiving and inversing an output signal of the fourteenth inverter;

a sixteenth inverter for receiving and inversing an output signal of the fifteenth inverter;

a seventeenth inverter for receiving and inversing an output signal of the sixteenth inverter and outputting a periodic signal to the NOR gate;

a eighteenth inverter for receiving and inversing an output signal of the sixteenth inverter;

a nineteenth inverter for receiving and inversing an output signal of the eighteenth inverter;

a twentieth inverter for receiving and inversing an

output signal of the nineteenth inverter; and

a twenty-first inverter for receiving and inversing an output signal of the twentieth inverter and thereon outputting to the second NAND gate.

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